

KATIKALA SOWMYA RANI

ELECTRONICS & COMMUNICATION ENGINEERING GRADUATE | EMBEDDED SYSTEMS | VLSI | ELECTRONICS HARDWARE

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SUMMARY

2026 Electronics and Communication Engineering graduate with a strong foundation in digital and analog electronics, microprocessors, microcontrollers, embedded systems, PCB design, and VLSI fundamentals. Hands-on exposure to Cadence Virtuoso, MATLAB, LabVIEW, Proteus, Xilinx Vivado, Arduino, 8051, Keil uVision, AutoCAD, and Fusion 360, with programming knowledge in C/C++, Python, and Java. Familiar with circuit design, simulation, hardware testing, troubleshooting, and technical documentation. Seeking an entry-level opportunity in Embedded Systems, Electronics Hardware, PCB Design, IoT, VLSI, or Testing

EDUCATION

Bachelor of Technology, Electronics and Communication Engineering 2022 — 2026
MLR Institute of Technology · CGPA: 7.87/10

Higher Secondary Education 2020 — 2022
St. Francis Juniour College for Women · CGPA: 7.86/10

Secondary Education 2020 — Present
CMR Model High School · 10/10

TECHNICAL SKILLS

Analog Circuits	Digital Electronics	Digital Systems
Electronic Devices	Microprocessors	Microcontrollers
CMOS Fundamentals	Arduino	Arduino IDE
8051 Microcontroller	Keil uVision	Embedded Systems Fundamentals
VLSI Design Fundamentals	CMOS Design	SRAM Design
Xilinx Vivado	PCB Design	Circuit Design
Circuit Simulation	Hardware Testing	Soldering
Cadence Virtuoso	MATLAB	LabVIEW
Proteus	AutoCAD	Fusion 360
C	C++	Python
Java	HTML	Microsoft Word
Microsoft PowerPoint	Technical Documentation	Presentations

PROJECTS

Design of an 8×8 SRAM Array using 10T Cell in 90nm Technology

Cadence Virtuoso | CMOS/VLSI Design

- Designed and implemented a 8×8 array using a 10T cell in 90nm technology.
- Applied digital design concepts to develop and test the proposed architecture.
- Performed analyzed simulation results to validate the design.
- Documented the design methodology, implementation, and results.

Analysis of 16x16 SRAM Array employing 7T and 10T Cells in 90nm Technology

Cadence Virtuoso | SRAM | CMOS Design

- Developed 16x16 SRAM Array with 7T and 10T Cells.
- Implemented using Cadence Virtuoso and evaluated system performance under different conditions.
- Strengthened practical understanding of digital systems, hardware design, and problem-solving.

RELEVANT COURSEWORK

- Digital Electronics
- VLSI Design
- CMOS Design
- Electronic Devices & Circuits
- Microprocessors & Microcontrollers
- Computer Architecture
- Semiconductor Devices

INTERNSHIP AND HACKATHON EXPERIENCE

- Participated in the Inventron Hackathon, collaborating with team members to develop and present a technical solution.
- Applied engineering knowledge, problem-solving, and analytical thinking during the hackathon.
- Gained experience working under time constraints and contributing to a team-based technical project.
- Participated in Smart India Hackathon (SIH) 2023 as part of a team working on a Wind Turbine-based project.
- Contributed to the development and technical discussions related to the project.
- Collaborated with team members to analyze the problem statement and work toward a technical solution.
- Gained experience in teamwork, problem-solving, technical presentation, and working under time constraints.
- Attended a hands-on workshop focused on AI tools and their practical applications.
- Gained exposure to using AI tools to support productivity, problem-solving, and technical tasks.
- Exposure to AI-assisted presentations, data analysis, coding, and debugging.